

Pub. No. 2002-100502

\* NOTICES \*

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

---

## CLAIMS

---

[Claim(s)]

[Claim 1] The surface mounting mold chip network components with which the network circuits which have three or more terminals [ odd ] are the surface mounting mold chip network components which it comes to form in even insulating-substrate sides, and said terminal is characterized by carrying out same number arrangement, respectively at the verge which said insulating substrate faces.

[Claim 2] The surface mounting mold chip network components characterized by being arranged at the insulating-substrate verge of the point symmetry location where the network circuits which have three or more terminals [ odd ] are the surface mounting mold chip network components which it comes to form in even insulating-substrate sides, and said terminal made said insulating-substrate side core center of symmetry, respectively.

[Claim 3] The surface mounting mold chip network component according to claim 1 or 2 characterized by the verge on which many terminals of the network circuit where it is formed and all network circuits adjoin each other so that it may have a terminal in each verge of two sides which the pair of an insulating substrate faces are arranged turning

into another verge.

[Claim 4] The surface mounting mold chip network component according to claim 3 characterized by being a terminal corresponding to the network circuit of equivalence where surface mounting mold chip network components consist of a network circuit group of the network circuit of the equivalence of a pair or two pairs, four pairs, eight pairs, or 16 pairs of equivalence, and all terminals serve as a pair in the point symmetry location which made the insulating-substrate side core center of symmetry.

[Claim 5] The surface mounting mold chip network component according to claim 1 to 4 characterized by including the network circuit where the circuit element was formed in insulating-substrate both sides one or more.

---

[Translation done.]

\* NOTICES \*

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

---

## DETAILED DESCRIPTION

---

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to surface mounting mold chip network components.

[0002]

[Description of the Prior Art] About the surface mounting mold chip network

components with which it comes to form in an insulating-substrate side the network circuit which has nine terminals (odd pieces), JP,4-165603,A has the indication. Five four are matched with the terminal for the verge which an insulating substrate faces in this official report ( drawing 3 ).

[0003]

[Problem(s) to be Solved by the Invention] It passes through the process (reflow process) connected [ which connect, and carries out a temperature up to the temperature which it is allotted so that cream solder may connect the land of the terminal area of surface mounting components, and a printed-circuit board, in case surface mounting components are mounted in a printed-circuit board etc. and a mounting object is formed, and the solder concerned fuses, is made to cool to a room temperature gradually after that, and combines ] mechanically [ said terminal area and a land / in solder ] and electrically.

[0004] In the process of the above-mentioned reflow process, the fused solder secures in the above-mentioned terminal area front face and the above-mentioned land front face the good condition of getting wet, and has low viscosity. Therefore, the force which pulls said each other's terminal area and said land with the surface tension of the fused solder works. so, at the reflow process of surface mounting die parts of coming to form in an insulating-substrate side the network circuit which has odd terminals as shown in drawing 3 Said tensile force of the side veranda of an insulating substrate with many terminals compares with said tensile force of the side veranda (reverse side) of an insulating substrate with few terminals. Since only a part with many terminals is strong, The melting solder of the verge by the side of the reverse concerned is cut off, and surface mounting die parts are considered to be easy to cause the so-called TSUMU stone phenomenon of said tensile force turning the verge of the strong one down, and starting.

[0005] Then, the technical problem which this invention tends to solve is controlling a TSUMU stone phenomenon in the surface mounting mold chip network components with which it comes to form in an insulating-substrate side the network circuit which

has three or more terminals [ odd ].

[0006]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, even of said network circuit are formed in the 2nd page of an insulating substrate, and the 1st configuration of the surface mounting mold chip network components with which it comes to form in the 2nd page of an insulating substrate the network circuit which has three or more terminals [ odd ] 1 of this invention is characterized by carrying out same number arrangement of the terminal 1 at the verge which an insulating substrate 2 faces, respectively.

[0007] If the surface mounting mold chip network components shown in drawing 1 are taken for an example, the number of the terminals 1 which each network circuit has is five, and two of these network circuits are formed in the 2nd page of an insulating substrate. Five verge which faces each other since an insulating substrate 2 is a rectangle is arranged in each long side which faces zero piece at a time those with 2 set, and the shorter side which faces each other, respectively, respectively.

[0008] If the surface mounting mold chip network components shown in drawing 2 are taken for an example, the number of the terminals 1 which each network circuit has is five, and this network circuit is formed in two fields of an insulating substrate 2. Four verge which faces each other since an insulating substrate 2 is a rectangle is arranged in each long side which faces one piece at a time those with 2 set, and the shorter side which faces each other, respectively, respectively.

[0009] It is shown that the notation (A, B, C, D) of the same kind given to four corners of drawing 1 , drawing 2 , insulating-substrate 2 front face of drawing 3 , and a rear face here is the location which corresponded with the front face and the rear face, respectively.

[0010] Since it becomes equal omitting the balance of the force which pulls the terminal 1 section and said each other's land by having the 1st configuration of the above at each verge, a TSUMU stone phenomenon can be controlled.

[0011] The 2nd configuration of the surface mounting mold chip network components

with which it comes to form in the field of an insulating substrate 2 the network circuit which has three or more terminals [ odd ] 1 of this invention for solve the above-mentioned technical problem is characterize by to be arrange at the verge of the insulating substrate 2 of the point symmetry location where even of said network circuit were formed in the 2nd page of an insulating substrate , and the terminal 1 made the core of the field of an insulating substrate 2 center of symmetry , respectively .

[0012] If the surface mounting mold chip network components shown in drawing 1 and drawing 2 are taken for an example, the number of the terminals 1 which each network circuit has is five, and this network circuit is formed in two insulating-substrate sides. Since the insulating substrate 2 here is a rectangle, the 2nd page core of an insulating substrate serves as the point that the two diagonal lines in the rectangle concerned cross, and it is arranged at the verge of the insulating substrate 2 of the point symmetry location where the terminal 1 made the field core of an insulating substrate 2 center of symmetry, respectively.

[0013] Since it becomes equal by the insulating-substrate 2 whole and the surface mounting mold chip network entire component omitting the balance of the force which pulls the terminal 1 section and each other's above-mentioned land by having the 2nd configuration of the above, a TSUMU stone phenomenon can be controlled.

[0014] The number of the terminals 1 in which the resister network circuit which has the common terminal of several nine terminals 1 as shown in drawing 3 other than several five partial pressure circuits of the terminal 1 which showed the example of the network circuit in the 1st and 2nd configuration of the above to drawing 1 , the capacitor element which are other circuit elements, and the inductor component were included is odd various filter circuits etc.

[0015] In order to solve the above-mentioned technical problem, the 3rd configuration of the surface mounting mold chip network components with which it comes to form in the field of an insulating substrate 2 the network circuit which has three or more terminals [ odd ] 1 of this invention In the 1st configuration of the above, and the 2nd configuration all network circuits It is the configuration characterized by the terminal 1

of the network circuit where the verge on which it is formed in so that it may have a terminal in each verge of two sides which the pair of an insulating substrate 2 faces, and many terminals 1 of each network circuit are arranged adjoins each other serving as verge other than the verge allotted. [ many ]

[0016] The example of the configuration of the above 3rd is shown in drawing 1 . It is formed and drawing 1 has the composition that the verge on which many terminals of an adjacent network circuit are arranged turns into another verge so that a network circuit [ all (two) ] may have a terminal 1 in each verge of two sides which the pair of an insulating substrate 2 faces. That is, the terminal 1 of the network circuit (right-hand side of drawing 1 "a front face") where the verge (verge ranging from the corner A to Corner B in drawing 1 ) on which many terminals 1 of each (for example, left-hand side of drawing 1 "a front face") network circuit are arranged adjoins each other serves as verge (verge ranging from the corner C to Corner D in drawing 1 ) allotted with the configuration used as another verge which faces each other. [ many ]

[0017] In the 3rd configuration of the above, it is desirable that it is the terminal 1 corresponding to the network circuit of equivalence where surface mounting mold chip network components consist of a network circuit group of the network circuit of the equivalence of a pair or two pairs, four pairs, eight pairs, or 16 pairs of equivalence, and all the terminals 1 serve as a pair in the point symmetry location which made the 2nd page core of an insulating substrate center of symmetry ( drawing 1 , drawing 2 ). The reason is to be able to permit mounting which rotated 180 degrees along the chip side, and for the burden of the components check at the time of the assembly activity of the electronic equipment using the surface mounting mold chip network components of this invention etc. to decrease.

[0018] The reason for having made the upper limit of the number of the network circuits of the above-mentioned equivalence into 16 pairs is because it is thought that a chip configuration becomes long and slender too much, and it is hard to maintain a mechanical strength, when the network circuit exceeding it is formed into 1 chip. As for the number of the network circuits of the viewpoint to the above-mentioned

equivalence, it is still more desirable that it is the pair shown in drawing 1 and drawing 2 , or they are two pairs.

[0019] With the network circuit group of the two above-mentioned pairs, four pairs, eight pairs, or 16 pairs of equivalence, when each pair consists of a circuit of equivalence and contrasts one pair and a pair different from it, what it may be equivalent or may be different species is pointed out.

[0020] Moreover, in the 1st, 2nd, and 3rd configuration of the above, it is desirable to include the network circuit where the circuit element was formed in insulating-substrate 2 both sides one or more. The reason is because effective use of the 2nd page of an insulating substrate is attained.

[0021] It is thought that effective use of the above-mentioned insulating-substrate side is effectiveness which is easy to be acquired by this invention primarily. For example, if drawing 1 and drawing 3 are compared simply, in drawing 3 , the field equivalent to it does not exist in drawing 1 to it being clear that insulating-substrate 2 corner A and near corner B are useless fields. This is said to be the fate of chip-like electronic parts of having odd terminals 1, and it originates in the ability of no terminals 1 to be arranged to two verge which a chip faces in a right-angle parallel location.

[0022] Moreover, generally as for the network circuit which has three or more terminals [ odd ], the circuitry itself becomes complicated in many cases. In that case, it is thought that there is an advantage which can control the electrical connection (short circuit) of the circuit elements contrary to a design intention by allotting each circuit element (resistance element) in one network circuit to insulating-substrate 2 both sides as shown in drawing 1 and drawing 2 .

[0023]

[Embodiment of the Invention] Hereafter, the gestalt of operation of the surface mounting mold chip network components of drawing 1 of this invention for an example is explained. The slit for division is prepared in all directions, the conductive paste which consists of silver system metal glaze is screen-stenciled and calcinated to one large-scale field of the insulating substrate 2 made from an alumina used as the

configuration of the insulating substrate 2 shown in drawing 1 after division, and a terminal 1 and a conductor are formed in it so that it may become like drawing 1 R> 1. Said screen-stencil is actuation while carrying out inhalation of air from the rear-face side of the large-sized insulating substrate 2, is that the conductive paste in a through hole and a corresponding location is absorbed into a through hole, and is considered as the so-called through hole printing made to adhere to a through hole internal surface. Moreover, the electrode used as a terminal 1 is formed in the location in which said electrode was formed in the opposite field of the insulating substrate 2, and the location which counters, respectively by this technique. Thereby, the electrode used as the terminal of insulating-substrate 2 both sides flows via a through hole internal surface.

[0024] Using the mask which has opening of resistor 3 configuration after that, ruthenium oxide system resistive paste is screen-stenciled so that it may be drawing 1, and it is calcinated, and a resistor 3 is formed. Subsequently, a HOU lead silicate system glass paste is screen-stenciled, calcinated and formed so that the resistor 3 whole may be covered (not shown). After that, for resistance adjustment, trimming by laser radiation is carried out so that it may become target resistance.

[0025] And the overcoat paste (not shown) of an epoxy resin system is screen-stenciled, and the paste concerned is stiffened so that the resistor 3 of insulating-substrate 2 both sides and glass may be covered at least and a terminal 1 may be slightly exposed.

[0026] Through that account division process of Gokami, nickel plating and solder plating can be further performed to the part of a terminal 1 at this order, and the surface mounting mold chip network components of this invention can be obtained. The terminal 1 by the side of the rear face of an insulating substrate 2 is contacted by mounting substrate sides, such as a printed circuit board, here at the time of mounting.

[0027] the process of the surface mounting mold chip network components of drawing 2 -- the process of the surface mounting mold chip network components of drawing 1 -- abbreviation -- it is the same. A different point is a mask opening location used at the time of the configuration (through hole location) of an insulating substrate, and



screen-stencil. Therefore, according to the process of the above-mentioned surface mounting mold chip network components of drawing 1 , the surface mounting mold chip network components of drawing 2 can be manufactured.

[0028] If two so-called partial pressure circuits of equivalence are both formed independently into 1 chip and drawing 1 and the surface mounting mold chip network components of drawing 2 are not mistaken even in the front flesh side of a chip, they have the structure where mounting to the printed circuit board in the condition that 180 degrees rotated along the chip side etc. is permissible. Therefore, it is desirable to carry out [ perform / printing or the notation which the color of the above-mentioned overcoat paste of a front flesh side is changed, and enable it to recognize the front flesh side of a chip simply, or can recognize the front flesh side of a chip easily on the overcoat front face of chip one side ]. Since the latter needs a printing process to the former not needing a printing process here, the ease of manufacture to the former is still more desirable.

[0029] It is thought that the surface mounting mold chip network components of drawing 2 can shorten some \*\*\*\*\* of the direction of a long side as compared with the surface mounting mold chip network components of drawing 1 . Although it depends also on a surface mounting mold chip network components user's design concept, if it asks for high density assembly, it will be thought that the surface mounting mold chip network components of drawing 2 are more advantageous.

[0030] in addition, the conductor in this example — although the film (a terminal 1, conductor), resistor 3 film, and glass membrane were formed by the screen-stencil which is the thick-film technique of excelling in mass-production nature, they may be formed by thin film technologies, such as sputtering, vacuum evaporation, and CVD. Moreover, it is good for insulating-substrate 2 top face (front face) also as a gestalt which has arranged partially as each circuit element separate electronic parts (the thing of a chip mold, the so-called discrete part, etc. are included) in all parts.

[0031] Although the conductive paste in this example was silver system metal glaze, it is replaced with it and can choose the electroconductive glue of silver content etc.

suitably.

[0032] Moreover, the resistor in this example can be suitably chosen according to the applications, such as a metal coat system and a carbon coat system, although it is a ruthenium oxide system. Moreover, although the HOU lead silicate system was used for the glass in this example, it is not limited to this. Moreover, it replaces with glass and a resin system can also be used. Moreover, in addition to this, the ingredient of an overcoat can also be suitably chosen according to the purposes, such as a resin system and a textile-glass-yarn ingredient, in addition to epoxy system resin.

[0033] Moreover, although based on laser radiation, the trimming method in this example is replaced with it, and can be suitably chosen according to the purposes, such as the sandblasting method.

[0034] Moreover, if the surface mounting mold chip network components of this invention can be constituted, the order of a process in this example can be changed. For example, it is forming a resistor 3 before formation of a conductor etc. Moreover, in this example, since the so-called through hole printing is adopted on the occasion of terminal 1 formation, the process which forms the so-called end-face electrode in the verge of an insulating substrate 2 is not included. However, in requiring the process, after the end face which should usually form an electrode in the division process in this example is exposed, an end-face electrode formation process is added before the above-mentioned plating process.

[0035] Moreover, although this example formed two terminals 1 in the verge by which each network circuit has five terminals 1, and faces three terminals 1 and the verge concerned at one verge of an insulating substrate 2 The effectiveness of this invention can be acquired by filling the conditions of the 1st configuration mentioned above or the 2nd configuration also with the case of a configuration of forming one terminal 1 in said one verge at four terminals 1, the verge concerned, and the verge that faces each other. That is, the mode of the arrangement in the insulating substrate 2 of odd terminals 1 is not limited to this example. Moreover, also about the number of the terminals 1 which each network circuit naturally has, it is not limited to five pieces but is good also as

three pieces, seven pieces, nine etc. pieces, etc.

[0036] Moreover, although the configuration of an insulating substrate 2 was made into the rectangle in this example, it replaces with it and various configurations, such as a square, a triangle, a hexagon, an octagon, and a round shape, can be adopted.

[0037] Moreover, although this example showed the partial pressure circuit as a network circuit which has three or more terminals 1, it is good also as a network circuit of others, such as the so-called CR network circuit which replaced with it and combined the resistance element and the capacitor element.

[0038]

[Effect of the Invention] By this invention, the network circuit which has three or more terminals [ odd ] was able to control the TSUMU stone phenomenon in the surface mounting mold chip network components which it comes to form in an insulating-substrate side.

---

[Translation done.]

\* NOTICES \*

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

---

DESCRIPTION OF DRAWINGS

---

[Brief Description of the Drawings]

[Drawing 1] It is the schematic diagram of the surface mounting mold chip network components of this invention.

[Drawing 2] It is the schematic diagram of the surface mounting mold chip network components of this invention.

[Drawing 3] It is the schematic diagram of the conventional surface mounting mold chip network components.

[Description of Notations]

1. Terminal
2. Insulating Substrate
3. Resistor

---

[Translation done.]

(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開2002-100502

(P2002-100502A)

(43) 公開日 平成14年4月5日 (2002. 4. 5)

(51) Int.Cl.<sup>7</sup>

識別記号

F I

テマコード<sup>\*</sup> (参考)

H 0 1 C 7/00

H 0 1 C 7/00

Z 5 E 0 3 3

H 0 1 G 4/40

H 0 1 G 4/40

3 0 7 A 5 E 0 8 2

審査請求 未請求 請求項の数 5 O L (全 6 頁)

(21) 出願番号 特願2000-285819 (P2000-285819)

(22) 出願日 平成12年9月20日 (2000. 9. 20)

(71) 出願人 500157837

ケイテックデバイシーズ株式会社

長野県上伊那郡箕輪町大字中箕輪14016番  
地30

(72) 発明者 小林 永司

長野県上伊那郡箕輪町大字中箕輪14016番  
30号 ケイテックデバイシーズ株式会社内

Fターム (参考) 5E033 AA02 AA18 AA22 BA01 BB02

BC07 BD11 BE01

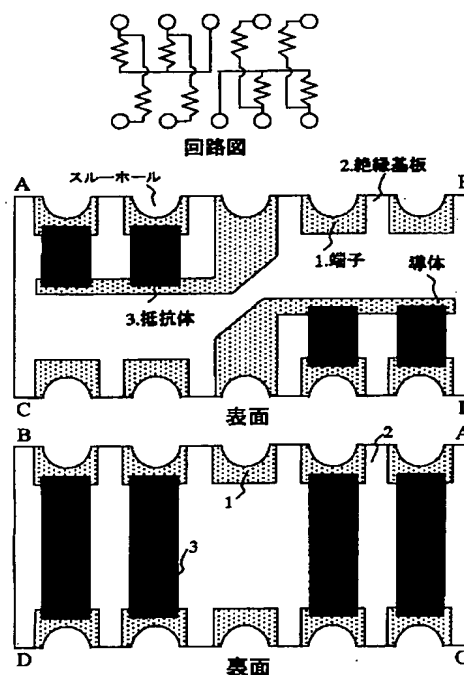
5E082 AA01 AB01 BC40 DD02 FG52

(54) 【発明の名称】 面実装型チップネットワーク部品

(57) 【要約】

【課題】 3以上の奇数個の端子を有するネットワーク回路が絶縁基板面に形成されてなる面実装型チップネットワーク部品において、ツームストーン現象を抑制する。

【解決手段】 ネットワーク回路が絶縁基板2面に偶数個形成され、且つ端子1が絶縁基板2の向かい合う辺縁にそれぞれ同数配置する。またネットワーク回路が絶縁基板2面に偶数個形成され、且つ端子1が、絶縁基板2の面の中心を対称の中心とした点対称位置の絶縁基板2の辺縁にそれぞれ配置する。



**【特許請求の範囲】**

【請求項1】 3以上の奇数個の端子を有するネットワーク回路が絶縁基板面に偶数個形成されてなる面実装型チップネットワーク部品であって、前記端子が、前記絶縁基板の向かい合う辺縁にそれぞれ同数配置されていることを特徴とする面実装型チップネットワーク部品。

【請求項2】 3以上の奇数個の端子を有するネットワーク回路が絶縁基板面に偶数個形成されてなる面実装型チップネットワーク部品であって、前記端子が、前記絶縁基板面中心を対称の中心とした点対称位置の絶縁基板辺縁にそれぞれ配置されることを特徴とする面実装型チップネットワーク部品。

【請求項3】 全てのネットワーク回路が、絶縁基板の一对の向かい合う2辺の辺縁それぞれに端子を有するよう形成され、

隣り合うネットワーク回路の端子が多く配される辺縁が、別の辺縁となることを特徴とする請求項1又は2記載の面実装型チップネットワーク部品。

【請求項4】 面実装型チップネットワーク部品が一对の等価のネットワーク回路、若しくは二対、四対、八対、又は十六対の等価のネットワーク回路群からなり、全ての端子が、絶縁基板面中心を対称の中心とした点対称位置にある対となる等価のネットワーク回路に対応した端子であることを特徴とする請求項3記載の面実装型チップネットワーク部品。

【請求項5】 絶縁基板両面に回路素子が形成されたネットワーク回路を1以上含むことを特徴とする請求項1～4のいずれかに記載の面実装型チップネットワーク部品。

**【発明の詳細な説明】****【0001】**

【発明の属する技術分野】 本発明は、面実装型チップネットワーク部品に関するものである。

**【0002】**

【従来の技術】 9つ（奇数個）の端子を有するネットワーク回路が絶縁基板面に形成されてなる面実装型チップネットワーク部品については、特開平4-165603号公報にその開示がある。同公報では、絶縁基板の向かい合う辺縁に端子が4つと5つ配されている（図3）。

**【0003】**

【発明が解決しようとする課題】 面実装部品が印刷回路板等に実装され、実装体を形成する際には、クリームはんだが面実装部品の端子部と印刷回路板のランドを繋ぐよう配され、当該はんだが溶融する温度まで昇温し、その後徐々に室温まで冷却させて前記端子部とランドとはんだで機械的、電気的に結合・接続させる工程（リフロー工程）を経る。

【0004】 上記リフロー工程の過程において、溶融したはんだは上記端子部表面と上記ランド表面とに良好な

濡れの状態を確保し、且つ低い粘性を有している。従って溶融したはんだの表面張力によって前記端子部と前記ランドとを引っ張り合う力が働く。そこで図3に示すような、奇数個の端子を有するネットワーク回路が絶縁基板面に形成されてなる面実装型部品のリフロー工程では、端子数の多い絶縁基板の辺縁側の前記引張力が端子数の少ない絶縁基板の辺縁側（逆側）の前記引張力に比して、端子数が多い分だけ強いいため、当該逆側の辺縁の溶融はんだが断ち切れ、面実装型部品が前記引張力が強い方の辺縁を下にして立ち上がる、いわゆるツームストーン現象を引き起こし易いと考えられる。

【0005】 そこで本発明が解決しようとする課題は、3以上の奇数個の端子を有するネットワーク回路が絶縁基板面に形成されてなる面実装型チップネットワーク部品において、ツームストーン現象を抑制することである。

**【0006】**

【課題を解決するための手段】 上記課題を解決するため、本発明の3以上の奇数個の端子1を有するネットワーク回路が絶縁基板2面に形成されてなる面実装型チップネットワーク部品の第1の構成は、前記ネットワーク回路が絶縁基板2面に偶数個形成され、且つ端子1が絶縁基板2の向かい合う辺縁にそれぞれ同数配置されていることを特徴とする。

【0007】 図1に示した面実装型チップネットワーク部品を例にとると、個々のネットワーク回路が有する端子1の数は5つであり、このネットワーク回路が絶縁基板2面に2つ形成されている。絶縁基板2は長方形であるため向かい合う辺縁は二組有り、向かい合う短辺にはそれぞれ0個ずつ、向かい合う長辺にはそれぞれ5個ずつ配置されている。

【0008】 図2に示した面実装型チップネットワーク部品を例にとると、個々のネットワーク回路が有する端子1の数は5つであり、このネットワーク回路が絶縁基板2の面に2つ形成されている。絶縁基板2は長方形であるため向かい合う辺縁は二組有り、向かい合う短辺にはそれぞれ1個ずつ、向かい合う長辺にはそれぞれ4個ずつ配置されている。

【0009】 ここで図1、図2、図3の絶縁基板2表面、裏面の4隅に付した同種の記号（A、B、C、D）は、表面、裏面でそれぞれ対応した位置であることを示している。

【0010】 上記第1の構成を有することにより、端子1部と前記ランドとを引っ張り合う力のバランスが各辺縁にて略均等になるため、ツームストーン現象を抑制することができる。

【0011】 上記課題を解決するための本発明の3以上の奇数個の端子1を有するネットワーク回路が絶縁基板2の面に形成されてなる面実装型チップネットワーク部品の第2の構成は、前記ネットワーク回路が絶縁基板2面に偶数個形成され、且つ端子1が、絶縁基板2の面の

中心を対称の中心とした点対称位置の絶縁基板2の辺縁にそれぞれ配置されることを特徴とする。

【0012】図1、図2に示した面実装型チップネットワーク部品を例にとると、個々のネットワーク回路が有する端子1の数は5つであり、このネットワーク回路が絶縁基板面に2つ形成されている。ここでの絶縁基板2は長方形であるため、絶縁基板2面中心は当該長方形における二本の対角線が交わる点となり、端子1が絶縁基板2の面中心を対称の中心とした点対称位置の絶縁基板2の辺縁にそれぞれ配置されている。

【0013】上記第2の構成を有することにより、端子1部と上記ランドとを引っ張り合う力のバランスが絶縁基板2全体、面実装型チップネットワーク部品全体で略均等になるため、ツームストン現象を抑制することができる。

【0014】上記第1、第2の構成におけるネットワーク回路の例は、図1に示した端子1の数5個の分圧回路の他に、図3に示すような端子1の数9個の、共通端子を有する抵抗ネットワーク回路や、その他の回路素子であるコンデンサ素子やインダクタ素子とを含ませた端子1の数が奇数個の各種フィルタ回路等である。

【0015】上記課題を解決するため、本発明の3以上の奇数個の端子1を有するネットワーク回路が絶縁基板2の面に形成されてなる面実装型チップネットワーク部品の第3の構成は、上記第1の構成及び第2の構成において、全てのネットワーク回路が、絶縁基板2の一对の向かい合う2辺の辺縁それぞれに端子を有するよう形成され、個々のネットワーク回路の端子1が多く配される辺縁が、隣り合うネットワーク回路の端子1が多く配される辺縁とは別の辺縁となることを特徴とする構成である。

【0016】上記第3の構成の具体例は、図1に示すものである。図1は全て(2つ)のネットワーク回路が、絶縁基板2の一对の向かい合う2辺の辺縁それぞれに端子1を有するよう形成され、隣り合うネットワーク回路の端子1が多く配される辺縁が、別の辺縁となる構成となっている。つまり個々(例えば図1「表面」の左側)のネットワーク回路の端子1が多く配される辺縁(図1中の隅Aから隅Bに亘る辺縁)が、隣り合うネットワーク回路(図1「表面」の右側)の端子1が多く配される辺縁(図1中の隅Cから隅Dに亘る辺縁)とは向かい合う別の辺縁となる構成となっている。

【0017】上記第3の構成において、面実装型チップネットワーク部品が一对の等価のネットワーク回路、若しくは二対、四対、八対、又は十六対の等価のネットワーク回路群からなり、全ての端子1が、絶縁基板2面中心を対称の中心とした点対称位置にある対となる等価のネットワーク回路に対応した端子1であることが好ましい(図1、図2)。その理由は、チップ面に沿って180°回転させた実装が許容でき、本発明の面実装型チ

ップネットワーク部品を用いる電子機器などの組立て作業時の部品チェック等の負担が低減するためである。

【0018】上記等価のネットワーク回路の数の上限を十六対にした理由は、それを上回るネットワーク回路を1チップ化すると、チップ形状が細長くなり過ぎ、機械的強度を維持しにくいと考えられるためである。その観点から、上記等価のネットワーク回路の数は図1、図2に示す一对であるか、又は二対であるのが更に好ましい。

【0019】上記二対、四対、八対、又は十六対の等価のネットワーク回路群とは、個々の対が等価の回路からなり、一つの対と、それと別の対を対比した場合、等価であっても異種であってもよいものを指す。

【0020】また上記第1、第2、第3の構成において、絶縁基板2両面に回路素子が形成されたネットワーク回路を1以上含むことが好ましい。その理由は絶縁基板2面の有効活用が可能となるためである。

【0021】上記絶縁基板面の有効活用は、そもそも本発明で得られ易い効果であると考えられる。例えば単純に図1と図3とを見比べると、図3では絶縁基板2隅部A、隅部B付近が無駄な領域であることが明らかであるのに対し、図1にはそれに相当する領域が存在しない。これは奇数個の端子1を有するチップ状電子部品の宿命とも言えることであり、チップの向かい合う2つの辺縁に全ての端子1を直角平行位置に配列できないことに起因している。

【0022】また3以上の奇数個の端子を有するネットワーク回路はその回路構成自体が一般的に複雑となる場合が多い。その場合図1、図2に示すように1つのネットワーク回路における個々の回路素子(抵抗素子)を絶縁基板2両面に配することで、設計意図に反した回路素子同士の電気接続(短絡)を抑制できる利点があると考えられる。

【0023】

【発明の実施の形態】以下、図1の面実装型チップネットワーク部品を例に、本発明の実施の形態を説明する。縦横に分割用のスリットが設けられ、分割後に図1に示す絶縁基板2の形状となる大型のアルミナ製の絶縁基板2の一方の面に、銀系メタルグレーズからなる導体ペーストをスクリーン印刷し、焼成して端子1及び導体を図1のようになるよう形成する。前記スクリーン印刷は、大型の絶縁基板2の裏面側から吸気しながらの操作であり、スルーホールと対応する位置にある導体ペーストがスルーホール内へ吸い込まれることで、スルーホール内壁面に付着させる、いわゆるスルーホール印刷とする。また絶縁性基板2の反対の面には前記電極を形成した位置とそれぞれ対向する位置に端子1となる電極を同手法で形成する。これにより、絶縁基板2両面の端子となる電極がスルーホール内壁面を経由して導通する。

【0024】その後抵抗体3形状の開口部を有するマス

クを用い、酸化ルテニウム系抵抗体ペーストを図1のようスクリーン印刷し、焼成して抵抗体3を形成する。次いで抵抗体3全体を覆うようにホウ珪酸鉛系ガラスペーストをスクリーン印刷し、焼成して形成する（図示しない）。その後抵抗値調整のため、目標とする抵抗値になるようレーザー照射によるトリミングを実施する。

【0025】そして絶縁基板2両面の抵抗体3、ガラスを少なくとも覆い、端子1がわずかに露出するよう、エポキシ樹脂系のオーバーコートペースト（図示しない）をスクリーン印刷し、当該ペーストを硬化させる。

【0026】その後上記分割工程を経て、更に端子1の部分にニッケルメッキ、はんだメッキをこの順に施し、本発明の面実装型チップネットワーク部品を得ることができる。ここで絶縁基板2の裏面側の端子1が印刷回路基板等の実装基板面に実装時に当接される。

【0027】図2の面実装型チップネットワーク部品の製法は、図1の面実装型チップネットワーク部品の製法を略同じである。異なる点は絶縁基板の形状（スルーホール位置）とスクリーン印刷時に用いるマスク開口部位置である。従って上記した図1の面実装型チップネットワーク部品の製法に準じて図2の面実装型チップネットワーク部品を製造できる。

【0028】図1、図2の面実装型チップネットワーク部品は、共にいわゆる等価の分圧回路が2つ独立して1チップ化されたものであり、チップの表裏さえ間違えなければ、チップ面に沿って180°回転した状態での印刷回路基板等への実装を許容できる構造となっている。従って表裏の上記オーバーコートペーストの色を異ならせて、チップの表裏を簡単に認識できるようにするか、チップ片面のオーバーコート表面にチップの表裏を簡単に認識できるような印字や記号を施す等するのが好ましい。ここで前者は印字工程を必要としないのに対し、後者は印字工程を必要とするため、製造の容易さから前者が更に好ましい。

【0029】図2の面実装型チップネットワーク部品は、図1の面実装型チップネットワーク部品に比して長辺方向の絶縁基板寸を多少短くできると考えられる。面実装型チップネットワーク部品使用者の設計思想にも依るが、高密度実装を求めるならば図2の面実装型チップネットワーク部品の方が有利と考えられる。

【0030】尚、本例での導体膜（端子1、導体）や抵抗体3膜やガラス膜は、量産性に優れる厚膜技術であるスクリーン印刷により形成したが、スパッタリング、蒸着、CVD等の薄膜技術によって形成しても良い。また絶縁基板2上面（表面）に別個の電子部品（チップ型のものや、いわゆるディスクリート部品等を含む）を各回路素子として部分的に、又は全箇所配置した形態としてもよい。

【0031】本例における導体ペーストは銀系メタルグレーズだったが、それに代えて銀含有の導電性接着剤等

を適宜選択し得る。

【0032】また本例における抵抗体は、酸化ルテニウム系だが、金属被膜系、炭素被膜系等その用途に合わせて適宜選択し得る。また本例におけるガラスにはホウ珪酸鉛系を用いたが、これに限定されない。またガラスに代えて樹脂系も使用できる。またオーバーコートの材料もエポキシ系樹脂以外にその他樹脂系やガラス系材料等目的に合わせて適宜選択し得る。

【0033】また本例におけるトリミング法は、レーザー照射によるものだったが、それに代えてサンドブラスト法等目的に合わせて適宜選択し得る。

【0034】また本発明の面実装型チップネットワーク部品を構成できるならば、本例における工程順を変更できる。例えば導体の形成前に抵抗体3を形成する等である。また本例では端子1形成に際して、いわゆるスルーホール印刷を採用しているため、絶縁基板2の辺縁にいわゆる端面電極を形成する工程が含まれていない。しかし、その工程を要する場合には、通常本例における分割工程において電極を形成すべき端面が露出した後、且つ上記メッキ工程前に端面電極形成工程が付加される。

【0035】また本例は個々のネットワーク回路が5つの端子1を有し、絶縁基板2の一つの辺縁に3つの端子1、当該辺縁と向かい合う辺縁に2つの端子1を形成したが、前記一つの辺縁に4つの端子1、当該辺縁と向かい合う辺縁に1つの端子1を形成する構成の場合でも、前述した第1の構成又は第2の構成の条件を満たすことで本発明の効果を得ることができる。つまり奇数個の端子1の絶縁基板2における配置の様子は本例に限定されない。また当然個々のネットワーク回路が有する端子1の数についても、5個に限定されず3個、7個、9個等としてもよい。

【0036】また本例では絶縁基板2の形状を長方形としたが、それに代えて正方形、三角形、六角形、八角形、円形等、種々の形状を採用し得る。

【0037】また本例では3以上の端子1を有するネットワーク回路として、分圧回路を示したが、それに代えて抵抗素子とコンデンサ素子を組み合わせ、いわゆるCRネットワーク回路等のその他のネットワーク回路としてもよい。

【0038】

【発明の効果】本発明により、3以上の奇数個の端子を有するネットワーク回路が絶縁基板面に形成されてなる面実装型チップネットワーク部品において、ツームストン現象を抑制することができた。

【図面の簡単な説明】

【図1】本発明の面実装型チップネットワーク部品の概略図である。

【図2】本発明の面実装型チップネットワーク部品の概略図である。

【図3】従来の面実装型チップネットワーク部品の概略



図である。

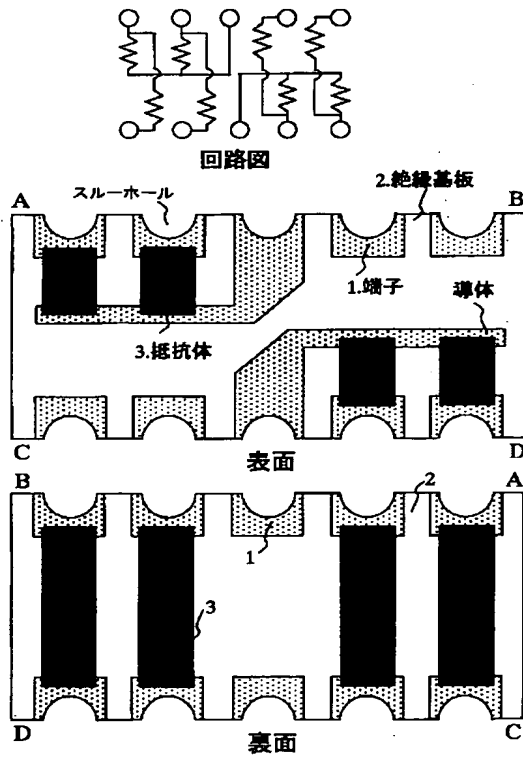
【符号の説明】

1. 端子

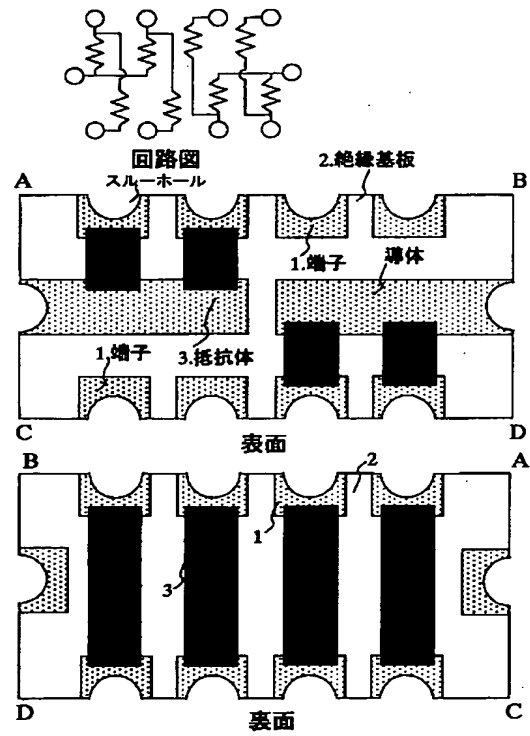
2. 絶縁基板

3. 抵抗体

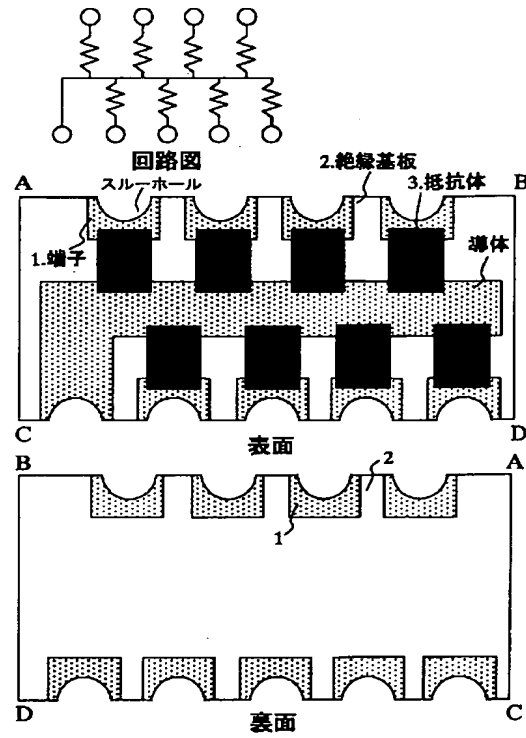
【図1】



【図2】



【図3】



**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

**BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**